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(81) Designated States *(national)*: CN, JP, KR.

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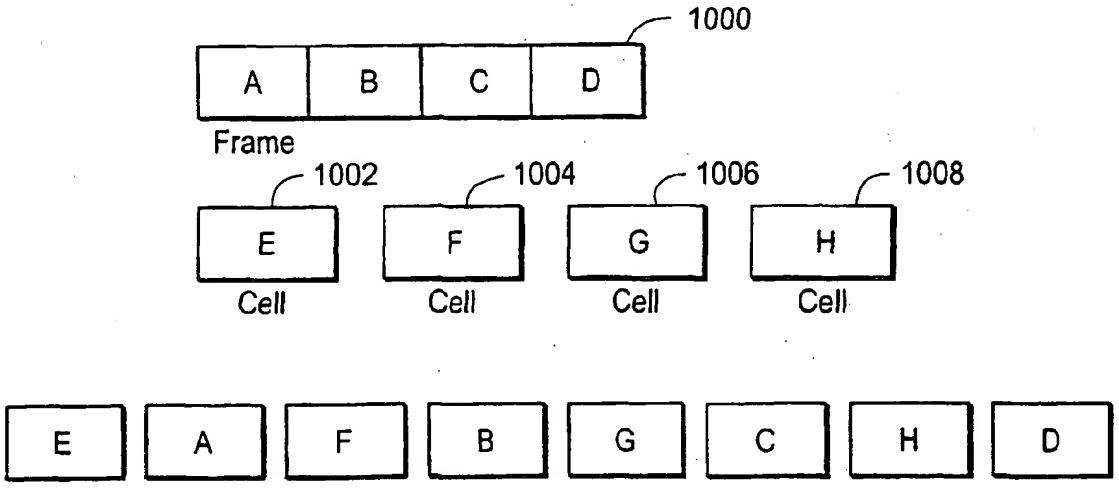
(54) Title: INTERLEAVEMENT FOR TRANSPORT OF FRAMES AND CELLS




(57) Abstract: A DMA system includes a plurality of transmit-receive pairs (102, 104) for communicating on a bus. A DMA controller (108) supervises bus handling. The DMA controller (108) includes a priority controller (114), a bus sniffer (112), and a context machine (116). The bus sniffer (112) and context machine (116) identify block transfers as frame or cell transfers and supervise interleaving. The priority controller (114) resolves the priority of each of the constituent transfers of the frame or cell block transfers using a matrix of priority tokens.

WO 02/15015 A2

# INTERLEAVEMENT FOR TRANSPORT OF FRAMES AND CELLS

## BACKGROUND OF THE INVENTION

### FIELD OF THE INVENTION

The present invention relates to data communication systems and, in particular, to an improved direct memory access (DMA) handler for an Internet Protocol (IP) over asynchronous transfer mode (ATM) system.

### DESCRIPTION OF THE RELATED ART

The Internet Protocol (IP) is one of the most popular networking protocols in use today. Briefly, IP encapsulates data into packets or frames of varying length. However, IP does not provide true quality of service (QoS), which is a requirement of multimedia messaging. Asynchronous transfer mode (ATM) systems pack data into equal length cells and also provide for true QoS.

Systems that employ IP over ATM must therefore provide for handling of the varying length IP frames and the fixed length ATM cells without doing violence to the ATM QoS requirements. One approach is to receive the IP frames, disassemble them, and reassemble them as ATM cells. This does not necessarily provide an optimal result, however.

As such, there is a need for an improved system for handling IP frames and ATM cells.

## SUMMARY OF THE INVENTION

These and other drawbacks in the prior art are overcome in large part by a direct memory access device (DMA) in accordance with the present invention. Briefly, the DMA device supports data transfers from multiple requestors over a shared media by interleaving frames and cells.

A DMA controller according to an implementation of the present invention includes a bus driver, a bus sniffer, a priority controller and a context machine. The bus sniffer is used to identify a cast type of a transfer on the bus, i.e., whether the transfer is a frame or cell transfer. The priority controller asserts a signal allowing access to the bus. The context machine stores system context. The controller supervises interleaving of frames and cells on the bus and asserts a frame end signal when a frame has been transmitted.

## BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the invention is obtained when the following detailed description is considered in conjunction with the following drawings in which:

FIG. 1 is a diagram illustrating interleaving of frames and cells according to an implementation of the present invention;

FIG. 2 is a block diagram of a processing system according to an implementation of the invention;

FIG. 3 is a diagram illustrating scan and service windows according to an implementation of the invention;

FIG. 4 is a diagram of an exemplary priority token matrix according to an implementation of the invention;

FIG. 5 is a diagram illustrating register stages according to an implementation of the invention;

FIG. 6 and FIG. 7 illustrate context assignment according to an implementation of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

FIGS. 1 – 7 illustrate an improved system and method for transporting frames and cells. A DMA system includes a plurality of transmit-receive pairs for communicating on a bus. A DMA controller supervises bus handling. The DMA controller includes a priority controller, a bus sniffer, and a context machine. The bus sniffer and context machine identify block transfers as frame or cell transfers and supervise interleaving. The priority controller resolves the priority of each of the constituent transfers of the frame or cell block transfers using a matrix of priority tokens.

FIG. 1A illustrates a frame 1000 and a plurality of cells 1002, 1004, 1006, 1008. The frame 1000 is of arbitrary length. As will be explained in greater detail below, a frame header includes frame length information, which is used to divide the frame into equal length elements A-D. The cells 1002, 1004, 1006, 1008 are of fixed length.

FIG. 1B illustrates interleavement of the frame and cells according to an implementation of the present invention. As will be described in greater detail below, a DMA controller according to an implementation of the present invention provides control signals to interleave the transmission of the frame elements A-D with the cells E-H.

Turning now to the drawings and, with particular attention to FIG. 2, a system 100 according to a particular implementation of the invention is shown therein and generally

identified by the reference numeral 100. As shown, the system includes a plurality of functional blocks 102, 104. As will be explained in greater detail below, each functional block 102, 104 includes a DMA bus interface 103a, 103b, respectively. In operation, one functional block 102 operates as a transmitter and another functional block 104 functions as a receiver. The transmit block and the receive block are referred to collectively as a transfer pair. Typically, the system 100 will include more than one transfer pairs, but only one is shown for sake of simplicity. Thus, the figure is exemplary only.

The system 100 further includes a bus 106 to which the functional blocks 102, 104 are coupled. The bus 102 may be implemented having source address 107a, destination address 107b, and data 107c channels.

Aiso coupled to the bus 106 is a DMA control unit 108 according to an implementation of the invention. The DMA control unit 108 includes a bus driver 110, a bus sniffer 112, a priority resolver 114, and a context machine 116, as will be explained in greater detail below.

More particularly, on the first transfer of a block transfer, the bus sniffer 112 reads the length field of the frame which is to be transferred, i.e., the parameters frame-length, frame-length descriptor position, and frame-length field size. A down-counter (not shown) is loaded by the frame-length value divided by the number of bytes which are transferred in parallel (i.e., the bus-width). The counter-value is decreased on each transfer. When the downcounter reaches zero (0), a frame-end signal is asserted.

The priority resolver 114 resolves concurrent transfer requests and grants transfer requests on a prereserved basis using tokens. The context machine 116 includes a plurality of registers and determines the associated response to each user data request. The driver 110 drives the bus 106 based on the register contexts. The bus sniffer 112 listens to the first transfer within a block transfer and determines the number of required transfers to complete the block transfer. At the end of the block transfer, the bus sniffer 112 asserts a frame-end signal.

As will be explained in greater detail below, the priority resolver 114 grants a transfer pair access to the bus on a per transfer basis, with a token assigned to each transfer. Thus, for example, with reference to FIG. 1B, each cell E-H and each frame element A-D represents a transfer and has assigned to it an associated token. The priority resolver 115 resolves the priority of any pending transfers. The context machine 116 is used to determine the specific handling of the component transfers of the block transfer(s).

As noted above, the function of the priority resolver 114 is based on „priority-tokens" and an assignment of „static rank" and „dynamic rank." Transfers are based on the use of the tokens in „scan windows" and „service windows." The tokens allow prereserving bus load share for each transfer-pair. More particularly, FIG. 3 illustrates the use of scan and service windows. Shown are a scan window 206 and a plurality of service windows 202a-202c. For each service window 202a-202c, a transfer service, based on the context information, occurs.

A service-window 202 is the time in which the dynamic rank is determined among all pending transfer-requesters. A scan-window 206 is a duration of time having a length equal to *n* service-windows 202 plus the duration of the performed transfer-services. Even if no requests are made during a service window 202, the service window period will elapse before a next one begins. Thus, each scan window 206 has a minimum duration of *n* service windows.

As will be explained in greater detail below, priority resolution itself is based on token assignment with reference to „static" and „dynamic" ranks. The static rank is based on a position within a matrix of n+1 (=rows) *m+1 (=columns). It is valid for a repitition of scan-window 206. The dynamic rank remains valid only within one service-window 202. Once the static ranking and dynamic ranking are determined, the corresponding transfer-requester is served based on its context-description. Each transfer leads to an „exhaustion" of the used token which will then only be „refreshed" at the beginning of the next scan-window.

Turning now to FIG. 4, a diagram of an exemplary token matrix is shown. Shown are a plurality of rows 401 and columns 403. The token-column is associated with the context-group of the potential transfer-requesters. Thus there are „m+1" context-groups. The token-rows are associated with the configuration registers of the priority resolver.

The figure depicts (n+1) configuration registers 403 (Level 2) with the register-size (m+1). They form in the logical sense the matrix for the priority tokens. According to one implementation of the present invention, there are three level of registers for the matrix (and two level for the remaining context). The registers at level 2 act as the main working registers; the register at level 0 and level 1 act as shadow-register stages. A device-embedded controller (not shown) sets a priority-token by writing a one to the respective bit-position of the register (Level 0)–the Most Significant Bit-positions of the register correspond with the context „m" as the Least Significant Bit-positions correspond with the context „0".

The Increase Address value 502e case can be used to increase either source address 506f, increase destination address 506g or increase both addresses 506h within a block-transfer. This can be used for fly-by tranfers in conjunction with directly bus-interfaced RAM-areas.

The Basic Source Address value 504b represents the Basic Source Address from which data will be transferred. To this address the offset is added.

The four different static offsets to Basic-Source Adress (BSA) 504b describe the statically added offset to the source-address from which data will be transferred.

The four different Destination Addresses 504c describe the addresses to which the data will be tranferred.

Two types of cast-types 504a are defined: cell transfer 506i and frame transfer 506j. As described above, when the frame transfer mode is used, the frame transfers are counted using the downcounter, and a frame end signal is asserted when the transfer is complete. The frame elements are then interleaved with cells on the bus, for example, using the prioity assignment described above.

The frame length field 506k expresses the frame-length. This information is required to determine when the frame-end signal shall be asserted.

The Frame-length Desriptor position field 506l provides a pointer to a total length or payload length field. More particularly, frame-based protocols (e.g. IP-v4 with the 2-Byte Total Length (TL) or IP-v6 also with a 2-Byte Payload length (PL) ) have a field which indicates the frame-length. This field provides a pointer to the beginning of this field to fetch TL/PL.

The frame-length field size field 506m describes the length of the frame length indicator (e.g. in the example listed above 2 Bytes). Offset is internally added to gain the appropriate counter-value.

The invention described in the above detailed description is not intended to be limited to the specific form set forth herein, but is intended to cover such alternatives, modifications and equivalents as can reasonably be included within the spirit and scope of the appended claims.

The registers 508 at Register Level 2 will start performing as the actual working-registers: Once it is determined that a request shall be granted, the corresponding bit is reset by the corresponding logic. All bits are refreshed at the end of the scan-window using the original configuration at Register Level 1. Then a new scan-window will start from the beginning.

As noted above, context machine 116 determines how the transfer is to be performed. Once a transfer request priority has been resolved, the context associated with the transfer is read. As shown in FIG. 6 and FIG. 7, a transfer request is serviced based on one of six main contexts 502a-f and several dynamically selected subcontexts 504a-d. The main contexts are bus share 502a, priority class 502b, listen-mode 502c, transfer size 502d, increase address 502e, and basic source address (BSA) 502f. The subcontexts are cast type 504a, and four each of static offsets to the basic source address 504b and destination addresses 504c.

The bus share context 502a has been described above and includes a plurality of settings (FIG. 7) to allow reservation of predetermined bus bandwidth.

According to the implementation illustrated, two priority contexts 502b are used: Standard 506a and preferred 506b. If standard 506a is used, the priority of a transfer-request will be granted on the basis of an available token with the highest dynamic rank, as described above.

If preferred 506b is used, bus-requests are immediately served. A transfer already started is not interrupted, but the use of the priority matrix does not apply. That means that until the very beginning of the next transfer, decisions based on priority-tokens could be overruled by the transfer-requester with „preferred"-context. If this mode is used one Priority-token less than „n" must be used for the matrix-initalization – the scan-window will remain the same.

Three listen mode values 502c are defined: OAM (Operations, Administration, and Maintenance)-listen 506c, Debug-Listen 506d, and OAM-Listen and Debug-Listen 506e. These signals can be used, e.g., to trigger a statistics-counter (not shown) or for debug-related operations.

OAM-Listen: On related transfers the signal OAM-listen will be asserted.

Debug-Listen: On related transfers the signal Debug-listen will be asserted.

OAM-Listen and Debug-Listen: On related transfers both signals will be asserted.

The transfer size value 506e specifies the block-transfer size, where „n" relates to the buswidth, i.e., how many bytes would be transferred by a single transfer.

The Increase Address value 502e case can be used to increase either source address 506f, increase destination address 506g or increase both addresses 506h within a block-transfer. This can be used for fly-by tranfers in conjunction with directly bus-interfaced RAM-areas.

The Basic Source Address value 504b represents the Basic Source Address from which data will be transferred. To this address the offset is added.

The four different static offsets to Basic-Source Adress (BSA) 504b describe the statically added offset to the source-address from which data will be transferred.

The four different Destination Addresses 504c describe the addresses to which the data will be tranferred.

Two types of cast-types 504a are defined: cell transfer 506i and frame transfer 506j. As described above, when the frame transfer mode is used, the frame transfers are counted using the downcounter, and a frame end signal is asserted when the transfer is complete. The frame elements are then interleaved with cells on the bus, for example, using the prioity assignment described above.

The frame length field 506k expresses the frame-length. This information is required to determine when the frame-end signal shall be asserted.

The Frame-length Desriptor position field 506l provides a pointer to a total length or payload length field. More particularly, frame-based protocols (e.g. IP-v4 with the 2-Byte Total Length (TL) or IP-v6 also with a 2-Byte Payload length (PL) ) have a field which indicates the frame-length. This field provides a pointer to the beginning of this field to fetch TL/PL.

The frame-length field size field 506m describes the length of the frame length indicator (e.g. in the example listed above 2 Bytes). Offset is internally added to gain the appropriate counter-value.

The invention described in the above detailed description is not intended to be limited to the specific form set forth herein, but is intended to cover such alternatives, modifications and equivalents as can reasonably be included within the spirit and scope of the appended claims.

**WHAT IS CLAIMED IS:**

1. A direct memory access controller, characterized by:

a bus sniffer (112) adapted to determine an end of a block transfer on a bus;

a priority control unit (114) adapted to guarantee bus share for transfer requests; and

a context machine (116) adapted to store request contexts for transfers on said bus;

wherein said priority control unit (114) is adapted to read a cast type of a context for each transfer and interleave asynchronous transfer mode (ATM) frames and Internet Protocol (IP) packets.

2. A direct memory access controller in accordance with claim 1, said priority control unit (114) adapted to determine a frame length prior to inserting said frame into a cell stream.

3. A direct memory access system, characterized by:

a bus (106);

a first functional block pair (102, 104) coupled to said bus and adapted to function as a receiver;

a second functional block pair (102, 104) coupled to said bus and adapted to function as a transmitter; and

a DMA controller (108) adapted to interleave transfers of ATM cells and IP frames between said first functional block pair and said second functional block pair on said bus.

4. A direct memory access system in accordance with claim 3, DMA controller (108) adapted to interleave said IP frames with ATM cells on a byte by byte basis.

5. A direct memory access system in accordance with claim 4, said DMA controller (108) adapted to assert an end of frame signal when a transfer is complete.

6. A direct memory access system in accordance with claim 5, said DMA controller (108) including a priority resolver (114) adapted to resolve priority based on

assignment of tokens.

7. A direct memory access system in accordance with claim 3, said DMA controller (108) including a down counter, wherein said down counter counts down for each transfer, a transfer being a number of bytes of said frame that can be transferred in parallel.

8. A direct memory access method, characterized by:

reading a cast type (504a), said cast type defining whether a transfer is a frame transfer or a cell transfer; and

determining a number of bytes of a frame cast type (506i) that can be transferred in parallel; and

transferring said number of bytes interleaved with cells of a cell transfer.

9. A method in accordance with claim 8, said transferring further comprising counting down from a number equal to a frame size divided by said number of bytes.

10. A method in accordance with claim 9, further comprising asserting an end of frame signal when said counter reaches a predetermined count.

11. A method in accordance with claim 10, comprising associating a priority token with each transfer of said number of bytes.

12. A direct memory access controller, characterized by:

means (102, 104, 108) for reading a cast type, said cast type defining whether a transfer is a frame transfer or a cell transfer;

means (102, 104, 108) operably coupled to said reading means for determining a number of bytes of a frame cast type that can be transferred in parallel; and

means (102, 104, 108) for transferring said number of bytes interleaved with cells of a cell transfer.

13. A controller in accordance with claim 12, said transferring further comprising means for counting down from a number equal to a frame size divided by said number of bytes.

14. A controller in accordance with claim 13, further comprising means for asserting an end of frame signal when said counter reaches a predetermined count.

15. A controller in accordance with claim 14, comprising means for associating a priority token with each transfer of said number of bytes.

16. A method, comprising:

providing a bus (106);

providing a first functional block (104) coupled to said bus and adapted to function as a receiver;

providing a second functional block (102) coupled to said bus and adapted to function as a transmitter; and

providing a DMA controller (108) adapted to interleave transfers of ATM cells and IP frames between said first functional block and said second functional block on said bus.

17. A method in accordance with claim 16, said DMA controller (108) adapted to interleave said IP frames with ATM cells on a byte by byte basis.

18. A method in accordance with claim 17, said DMA controller (108) adapted to assert an end of frame signal when a transfer is complete.

19. A method in accordance with claim 18, said DMA controller (108) including a priority resolver adapted to resolve priority based on assignment of tokens.

20. A method in accordance with claim 19, said DMA controller (108) including a down counter, wherein said down counter counts down for each transfer, a transfer being a number of bytes of said frame that can be transferred in parallel.

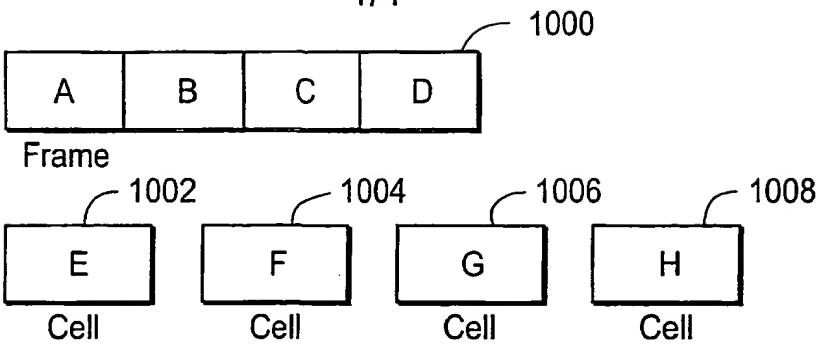



FIG. 1A


FIG. 1B

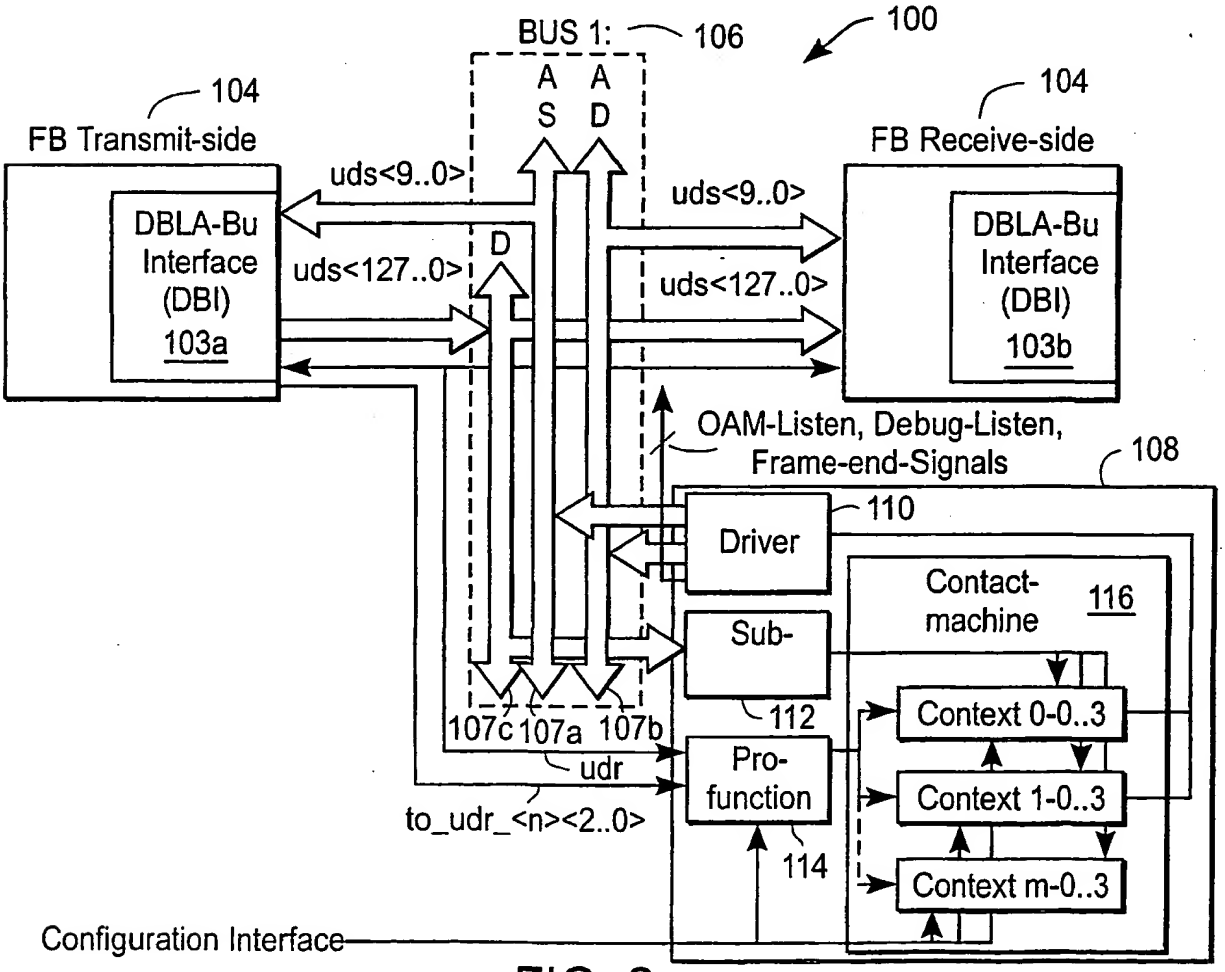



FIG. 2

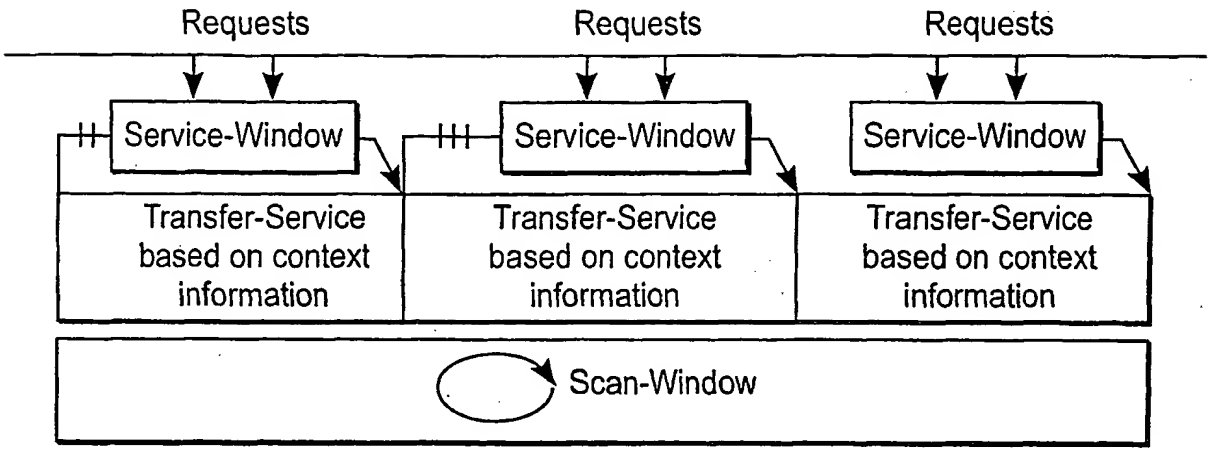



Figure time-relation of Service-Windows to transfers within Scan-Windows

FIG. 3

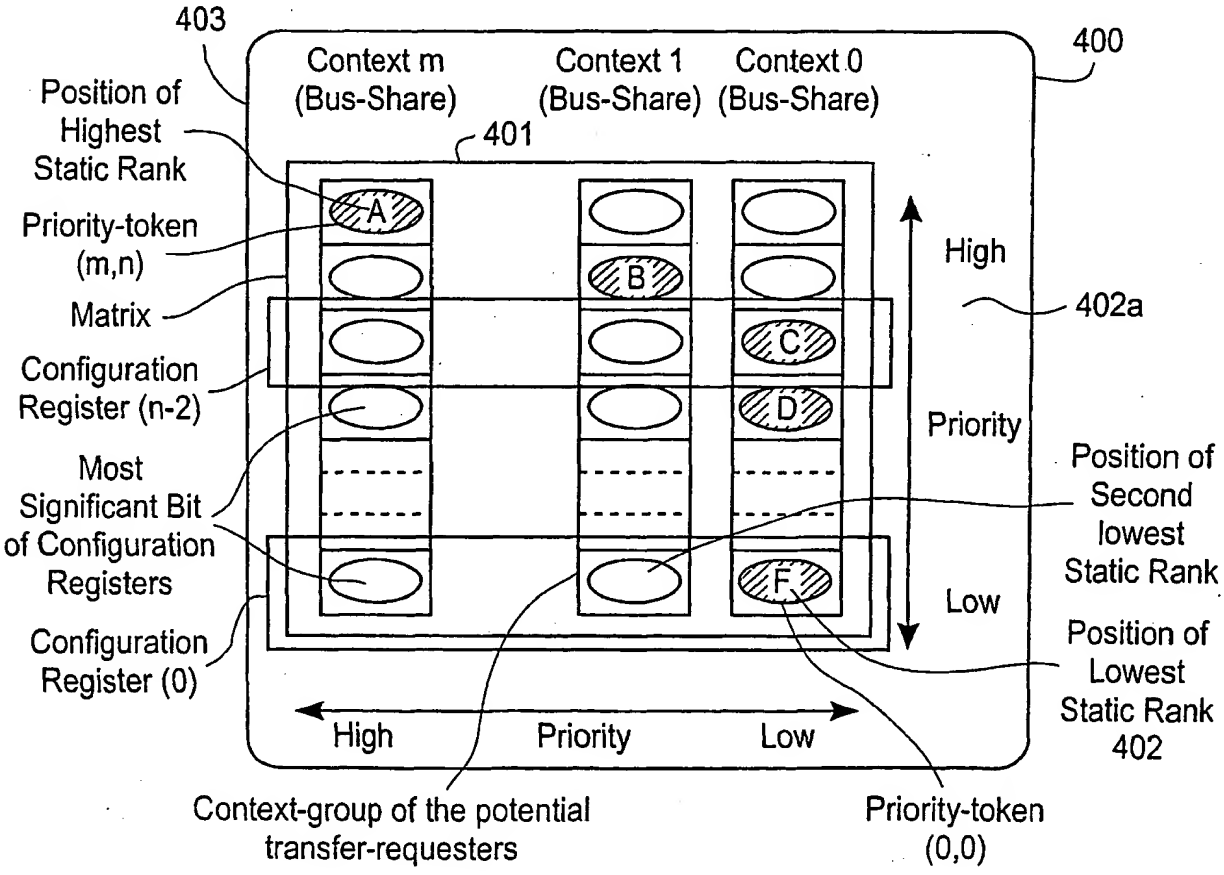



Figure Priority-token matrix overview

FIG. 4

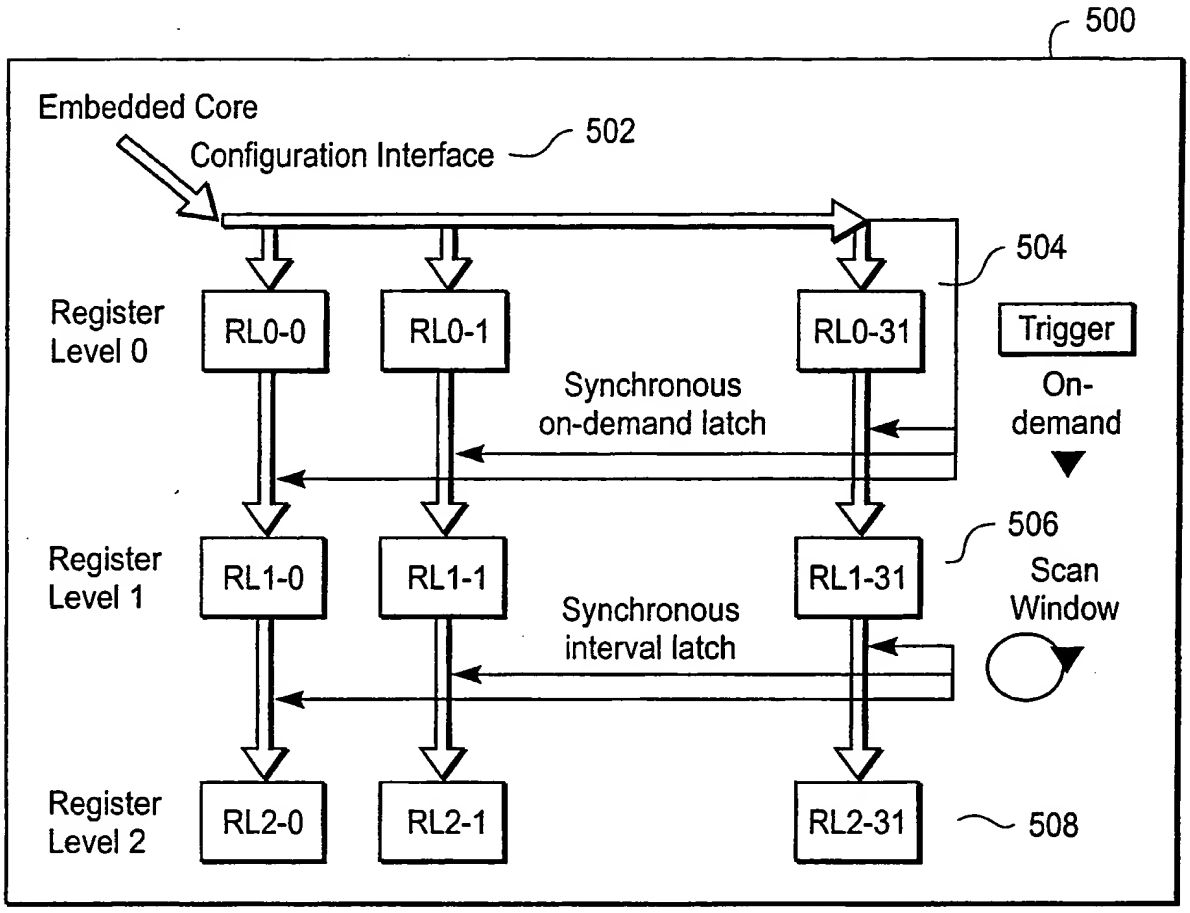



FIG. 5

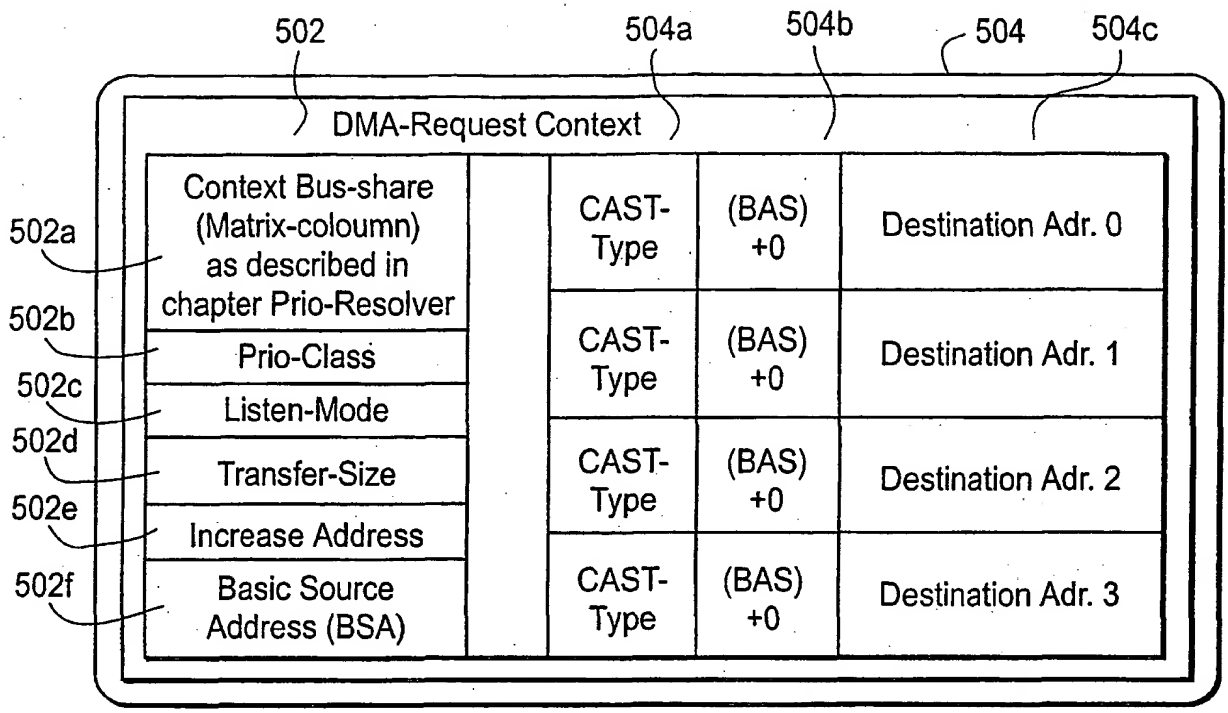



FIG. 6 figure DMA-Request Context

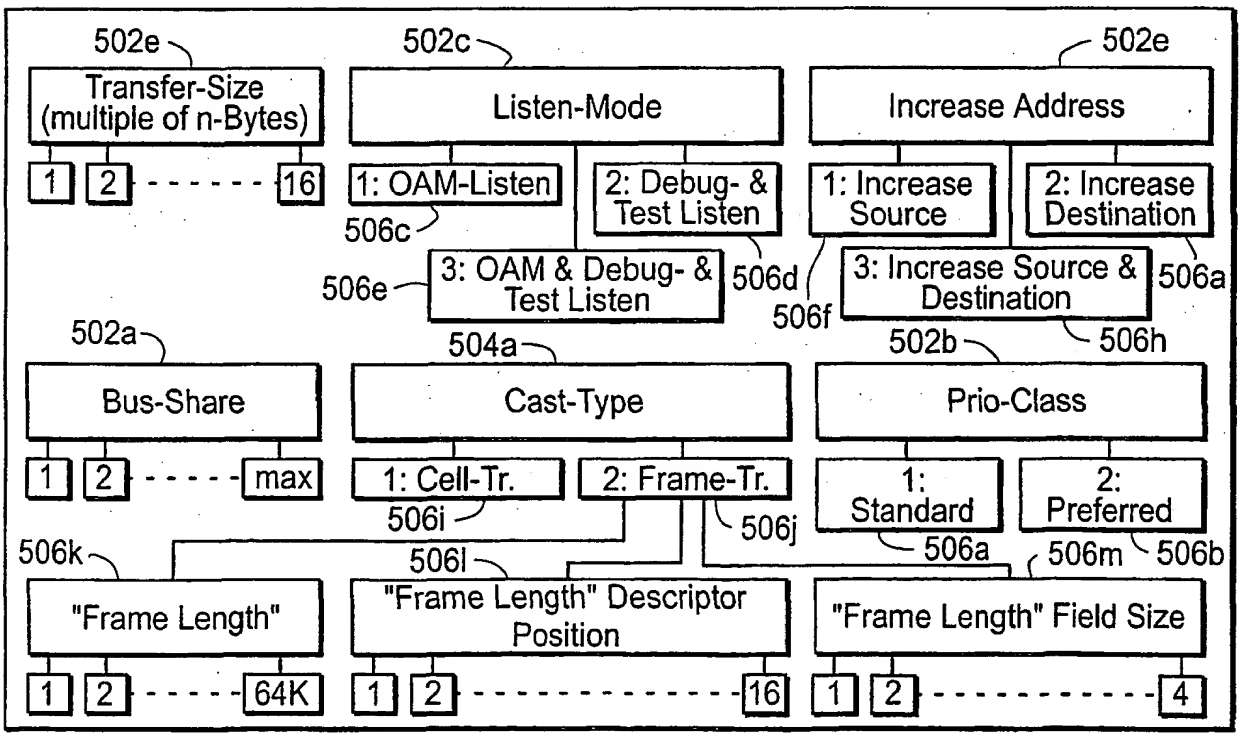



FIG. 7 figure Configuration-cases

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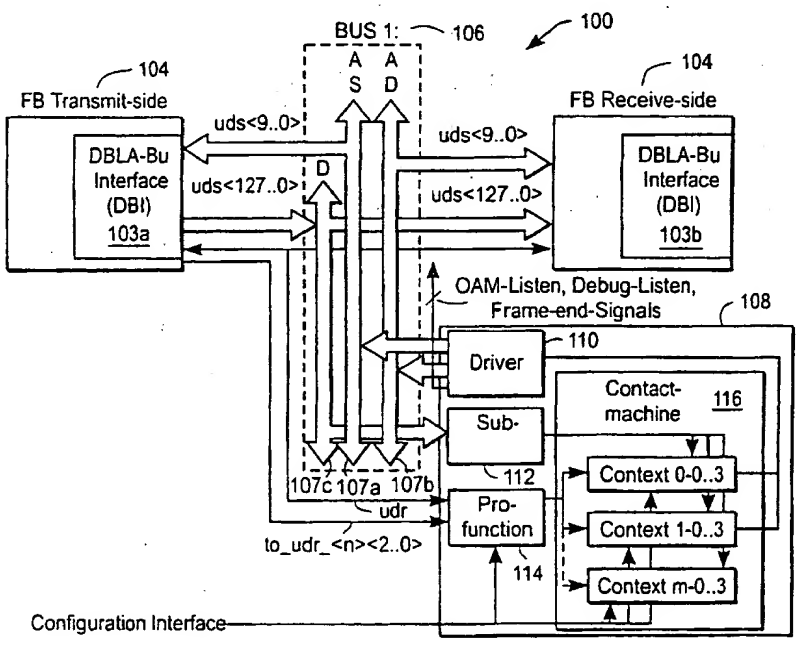


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# INT RNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F13/30 G06F13/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 5 659 749 A (MITCHELL BOB ET AL)<br>19 August 1997 (1997-08-19)<br>column 2, line 9 - line 51<br>--- | 1-20 |
| A | EP 0 550 164 A (SUN MICROSYSTEMS INC)<br>7 July 1993 (1993-07-07)<br>column 3, line 7 - line 31<br>claims 1,2,6,7<br>--- | 1-20 |
| P,A | EP 1 059 588 A (TEXAS INSTRUMENTS INC)<br>13 December 2000 (2000-12-13)<br>page 2, line 18 - line 42<br>page 3, line 45 - line 48<br>page 5, line 30 - line 32<br>page 5, line 50 - line 51<br>page 8, line 13 - line 29<br>page 16, line 36 - line 39<br>claims 1-3<br>---<br>-/-- | 1-20 |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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|---|---|
| 25 January 2002 | 05/02/2002 |

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|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax (+31-70) 340-3016 | Henneman, P |

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication,where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| P,A | US 6 115 373 A (LEA CHIN TAU)<br>5 September 2000 (2000-09-05)<br>the whole document | 1-20 |

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Information on patent family members

Inten..onal Application No
PCT/US 01/24205

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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